UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,286	06/27/2003	Abbas Ali	TI-31505A	8530

23494 7590 03/11/2005

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,286	ALI ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *062703*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The preliminary amendment filed on 6/27/2003 has been entered

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3 and 9 recites the limitation "second etch stop layer" in claims 1 and 7. There is insufficient antecedent basis for this limitation in the claims.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

GP

Claims 1-12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-12 of U.S. Patent No. 6,605,540 in view of Chao et al (US 6,429,119)

Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-12 of US 6,605,540 differ from claims 1-12 of the instant claimed invention by claiming the specific depth of the first trench and the second trench. Chao discloses a process for manufacturing a dual damascene comprises the steps of etching the first trench and the second trench to the specific depth (col 8, lines 20-48). One skilled in the art at the time the invention was made would have found it obvious to modify claims 1-12 of the instant claimed invention by etching the first trench and the second trench to the specific depth to produce the claims 1-12 of US 6,605,540 in view of Chao teaching because Chao discloses that the via/trench etch depth controlled by an endpoint trench etch stop layer and endpoint process control (col 8, lines 21-26)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Chao et al (US 6,429,119)

Chao discloses a process for manufacturing dual damascene. This process comprises the steps of:

providing a silicon substrate 10 containing conductive line 12 (col 7, lines 33-35; fig. 1) reads on providing a silicon substrate containing one or more electronic devices

forming a first dielectric layer 17 (oxide) over the substrate 10, layer 17 having a thickness/first thickness (col 7, lines 56-59; fig. 1)

forming a first etch stop layer 18 over dielectric layer 17/first dielectric layer (col 7, lines 66-67; fig. 1)

forming a second dielectric layer 19 over the first dielectric layer 17, layer 20 having a thickness (col 7, lines 10-12, fig. 1)

forming a silicon oxynitride layer 30 (claimed antireflective coating layer) over dielectric layer 19/second dielectric (col 8, lines 35-38 ;fig. 3)

etching a first trench 20 in the dielectric layer 19/second dielectric layer (col 8, lines 20-25)

etching at the same time a second trench 40 having a depth in the second dielectric layer 19 and a trench 44 in the first dielectric layer 17 (col 8, lines 45-50 and fig. 4, fig. 4 shows that the depth of second trench/second depth is approximately equal to the thickness of second dielectric layer 19

forming a contacting/conductive copper layer filling both first and second trenches (col 4, lines 52-55; col 8, lines 55-60)

The limitations of claim 2 has been discussed above

Regarding claim 3, Chao discloses that the stop layers are made of silicon nitride (col 8, lines 1-3)

5. Claims 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Chao et al (US 6,429,119)

Chao discloses a process for manufacturing dual damascene. This process comprises the steps of:

providing a silicon substrate 10 containing conductive line 12 (col 7, lines 33-35; fig. 1) reads on providing a silicon substrate containing one or more electronic devices

forming a first dielectric layer 17 (oxide) over the substrate 10, layer 17 having a thickness/first thickness (col 7, lines 56-59; fig. 1)

forming a first etch stop layer 18 over dielectric layer 17/first dielectric layer (col 7, lines 66-67; fig. 1)

forming a second dielectric layer 19 over the first dielectric layer 17, layer 20 having a thickness (col 7, lines 10-12, fig. 1)

forming a silicon oxynitride layer 30 (claimed antireflective coating layer) over dielectric layer 19/second dielectric (col 8, lines 35-38 ;fig. 3)

etching a first trench 20 to a depth/first depth in the second dielectric layer 19 and first dielectric layer 17 (col 8, lines 20-25; fig. 2 shows the depth is greater than the thickness of layer 19/second dielectric)

etching at the same time a second trench 40 having a depth in the second dielectric layer 19 and a trench 44 in the first dielectric layer 17 (col 8, lines 45-50 and fig. 4, fig. 4 shows that the depth of second trench/second depth is approximately equal to the thickness of second dielectric layer 19

forming a contacting/conductive copper layer filling both first and second trenches (col 4, lines 52-55; col 8, lines 55-60)

Regarding claim 8, Chao silicon oxynitride ARC layer 30 inherently has the atomic percent numbers as recited in claim 8 because the atomic percent numbers are physical properties of SiON (see prior art of record for evidence of this basis)

Regarding claim 9, Chao discloses that the stop layers are made of silicon nitride (col 8, lines 1-3)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4-5,10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al (US 6,429,119) in view of Krishnaraj et al (US 6,511,923).

Chao's method has been described above. Chao differs from the instant claimed inventions as per claims 4-5, 10-11 by forming the first and second dielectric layers of oxides instead of FSG (Fluorosilicate glass)

However,Krishnaraj, in a method of forming dual damascene,discloses replacing silicon oxide with FSG as intermediate dielectric (col 1, lines 23-25)

Hence, one skilled in the art would have found it obvious to substitute Hung oxide dielectric layer with FSG in view of Krishnaraj teaching because Krishnaraj discloses that FSG is an attractive solution to replace conventional silicon dioxide as intermetal dielectrics for damascene structures (col 1, lines 23-26)

8. Claims 6, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al (US 6,429,119) in view of Cheung et al. (US 6,348,725).

Chao's method has been described above. Unlike the instant claimed inventions as per claims 6, 12, Chao fails to disclose the step of forming a liner film in the first and second trench.

However, Cheung discloses a process of forming dual damascene comprises the step of forming a barrier/liner 524 in the first and second trench before filling the trench with conductive material (col 16, lines 46-48)

Hence, one skilled in the art would have found it obvious to modify Chao's method by adding the step of forming a barrier/liner in the first and second trench to prevent the migration of copper into the surrounding silicon and/or dielectric material as taught by Cheung (col 16, lines 47-49)

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sim et al (US 6,423,654) discloses that SiON has an atomic composition ratio of silicon (25-40%), oxygen (25-40%), nitrogen (25-40%) (abstract)

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
March 4, 2005